AMENDMENTS TO THE DRAWINGS

Applicants submit herewith a replacement sheet for Sheet 1 providing amendments to FIG. 1. The replacement sheets for sheets 2-4 include formal changes to the drawings and do not include any substantive changes.

REMARKS/ARGUMENTS

The arguments and amendments submitted herein incorporate the patentability arguments and amendments Applicants discussed with the Examiner during the phone interview. Applicants submit that the amendments and arguments presented herein make the substance of the phone interview of record to comply with 37 CFR 1.133. If the Examiner believes that further information on the interview needs to be made of record to comply with the requirements, Applicants request the Examiner to identify such further information.

During the interview, the Examiner said that the discussed amendments appear to distinguish over the cited art and that the rejection would be reconsidered in view of the amendments and arguments, which are presented herein.

In the Office Action, the Examiner said that Applicants elected Species 1 "without traverse." Applicants dispute this characterization and note that in the Response to Restriction Requirement dated September 11, 2006, Applicants traversed the restriction requirement with the election on page 1 of the Response.

The Examiner objected to the drawings and requested that Applicants include the operating system 8 and adapter device driver 14 in the memory 6 because such components run in memory. Applicants made the suggested amendments to FIG. 1 of the drawings to include these components 8 and 14 in the memory 6. Applicants submit that this Amendment overcomes the objection to the drawings.

The Examiner objected to FIG. 1 showing the adaptor device driver 14 as connected to the bus 11. Applicants corrected FIG. 1 to have the memory 6 including the device driver 14 connect to the bus because the adaptor device driver 14 executing in the memory 6 communicates over the buss 11. See, Specification, para. [0004], pg. 2.

Applicants submit that the amendments to FIG. 1 overcome the objections to the Specification and Drawings.

1. Amended Claim 25 is Directed to Statutory Subject Matter

The Examiner rejected claim 25 as directed to non-statutory subject matter (35 U.S.C. §101) on the grounds the claims may cover transmission media. (Office Action, pgs. 3-4) Although applicants traverse the legal basis of this finding, to expedite prosecution, Applicants amended claim 25 to recite that the article of manufacture comprises at least one of a hardware

device having hardware logic and a computer readable storage medium having computer executable code. These added requirements are disclosed on at least para. [0015], pgs. 6-7 of the Specification.

Applicants submit that this amendment overcomes the Section 101 rejection.

2. Claim 12 Complies With the Enablement Requirement

The Examiner rejected claim 12 finding that the claimed "circuitry" language did not comply with the enablement requirement of 35 U.S.C. §112, par. 1 on the grounds that the circuit refers to only software. (Office Action, pg. 4)

Applicants traverse and dispute this finding because the Specification specifically discloses that the:

> circuitry for performing the operations of the described embodiments may comprise a hardware device, such as an integrated circuit chip, Programmable Gate Array (PGA), Application Specific Integrated Circuit (ASIC), etc. The circuitry may also comprise a processor component, such as an integrated circuit, and code in a computer readable medium, such as memory, wherein the code is executed by the processor to perform the operations of the described embodiments.

Specification, para. [0016], pg. 7.

Thus, the Specification discloses that the circuitry for performing operations may comprise a hardware device and/or a processor component that executes code. Accordingly, the Examiner's finding that the Specification "refers to the circuit as being directed to as only software" is incorrect. Applicants submit that the term "circuitry" as used in the claims and defined in the Specification complies with the enablement requirement because the written description and use of the term "circuitry" in the Specification enables any person skilled in the art to make and use the same.

Accordingly, Applicants request that the rejection under Section 112, par. 1 be withdrawn.

3. Amended claims 2-6, 12-19, and 23-33 Comply with the Definiteness Requirement

The Examiner rejected claims 2-6, 12-19, and 23-33 as indefinite (35 U.S.C.§112, par. 2). Applicants traverse with respect to the amended claims.

Applicants amended claims 1-4, 6, 7, 8, 12-15, 17-19, 23-28, and 30-32 as discussed with the Examiner to clarify the language and overcome the indefiniteness rejections with respect to the claims.

In particular, the Examiner found that the use of the term "recent" in claim 3, as well as claims 14, and 27 was indefinite. (Office Action, pg. 5) Applicants amended these claims to remove the term "recent" to overcome this indefiniteness rejection.

The Examiner found claims 5, 16, and 29 indefinite because of the use of the term "at least one buffer". (Office Action, pg. 6) Applicants amended these claims to clarify "the buffer" to overcome this indefiniteness rejection.

Applicants amended claim 12 to clarify that the memory includes "a buffer" to overcome the indefiniteness rejection on pg. 6 of the Office Action. Applicants submit that the term "circuitry" in claim 12 is not indefinite as the Examiner contends on pg. 6 of the Office Action because the Specification provides a definition of "circuitry" as discussed above, as a hardware device and/or processor. Applicants submit that this term is definite for the reasons discussed above.

Applicants amended claim 20 to be a "system" claim that depends from claim 12 to overcome the antecedent basis rejection on pg. 7 of the Office Action.

Applicant submit that the indefiniteness rejection should be withdrawn in view of the amendments.

4. Claims 1, 4-7, 9, 12, 15-18, 20, 23, 25, 28-31, and 33

The Examiner rejected claims 1, 4-7, 9, 12, 15-18, 20, 23, 25, 28-31, and 33 as anticipated (35 U.S.C. §102(b)) by Baumert (U.S. Patent No. 6,067,300). Applicants traverse with respect to the amended claims.

Amended claims 1, 12, 23, and 25 require: receiving a first packet for a buffer in memory; generating a descriptor indicating a length of the first packet and a buffer address of the buffer; receiving at least one subsequent packet following the first packet; determining whether the buffer has available space to store the first packet and the at least one subsequent packet received before transferring the first and the at least one subsequent packet to the buffer; generating a descriptor for the first packet and the at least one subsequent packet indicating the buffer in response to the determining that the buffer has available space; transferring to the

buffer the first packet and the at least one subsequent packet capable of fitting into the buffer in response to the determining that the buffer has available space, wherein the descriptors for the first and the at least one subsequent packet indicate the same buffer while the first and the at least one subsequent packet are stored in the buffer; and adding the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.

Applicants amended these claims to add the determining requirement from claim 2 and to clarify that the determination of whether the buffer has available space occurs before the first and the at least one subsequent packet are transferred to the buffer and that the descriptor indicating the buffer is generated for the first packet and the at least one subsequent packet. Applicants further added the requirement that the transferring operation is performed in response to determining that the buffer has available space and that the descriptors for the first and the at least one subsequent packet indicate the same buffer while the first and the at least one subsequent packet are stored in the buffer. These added requirements are disclosed on at least pgs. 4-5 and FIGs. 3-4 of the Specification.

During the phone interview, the Examiner indicated the amendments made to the independent claims would likely overcome the cited Baumert and that he would update his search. Applicants further note that the Examiner did not cite any art with respect to the limitations of claim 2, including the limitation added to the independent claims.

The Examiner cited col. 1, lines 23-27 and 49-53, col. 3, lines 4-19, and col. 5, lines 13-36 and 27-60 with respect to the pre-amended independent claims. (Office Action, pgs. 7-8) Applicants traverse with respect to the amended claims.

The cited cols. 1 and 3 discuss controllers, a packet memory which stores data packets prior to transferring to another LAN and a descriptor memory storing pointers to the data packets. A switch controller defines a receive data path and a transmit data path for concurrently transferring data in both directions between the MACs and the packet memory. Nowhere do the cited cols. 1 and 3 anywhere disclose the claim requirements of determining whether a buffer has space to store a first packet and the at least one subsequent packet before transmitting them to the buffer. Further, nowhere do the cited cols. 1 and 3 anywhere disclose transferring to the buffer the first packet and the at least one subsequent packet in response to determining the buffer has available space or that the descriptors of the first and at least one subsequent packet indicate the

same buffer while they are store din the buffer. Instead, the cited cols. 1 and 3 discuss a packet memory and descriptors pointing to the packets in the memory.

The cited col. 5, lines 27-30 mentions that the received data packets are stored in one or more buffers within the packet memory. Although the cited col. 5 mentions that data packets are stored in one or more buffers, nowhere does this cited col. 5 anywhere disclose the claim requirements that multiple packets are transferred to one buffer at the same time, such that their descriptors indicate the same buffer while the first and the at least one subsequent packet are stored in the buffer. In fact, further cited Baumert teaches away from this claim requirement.

The cited col. 5 further mentions that "the size of the buffers 70 is selected such that the smallest size data packet, i.e., 64 bytes, can fit within a single buffer 70 while the largest size data packet .... will require a plurality of buffers." Thus, the cited col. 5 clarifies that one buffer is used for one packet. The Examiner has not cited any part of Baumert that discloses the claim requirements that multiple packets are transferred to one buffer in response to determining that the buffer has available space, where the determination is made before transferring the first and the at least one subsequent packet to the buffer, and where the descriptors of the first and the at least one subsequent packet indicate the same buffer while the packets are stored in such buffer.

Accordingly, for the above discussed reasons, Applicants submit that amended independent claims 1, 12, 23, and 25 are patentable over the cited art because the cited Baumert does not disclose all the claim requirements.

Claims 4-7, 9, 15-18, 20, 28-31, and 33 are patentable over the cited art because they depend from one of claims 1, 12, and 25, which are patentable over the cited art for the reasons discussed above. Moreover, the following dependent claims provide further grounds of patentability over the cited art.

Amended claims 4, 15, and 28 depend from claims 1, 12, and 25, respectively, and further require that the first and the at least one subsequent packets are transferred to the buffer in response to a timer expiring.

The Examiner cited the above discussed cols. 1, 3, and 5 of Baumert as teaching the transferring of a data packet into a buffer is done after a rising or falling of an edge of the clock within the system. The Examiner found this teaching discloses the requirements of the claims. (Office Action, pg. 8) Applicants traverse.

Applicants could not find any mention in the cited cols. 1, 3, and 5 of transferring a data packet into a buffer after a rising or falling of an edge of the clock. Col. 8, lines 40-57 of Baumert mentions that data is written into the packet memory at a different rate than it is written into the packet memory output buffer to accommodate different external and internal clock rates.

Applicants submit the Examiner has not cited any part of Baumert that discloses that the first and the at least one subsequent packets are transferred to the buffer in response to a timer expiring.

Accordingly, claims 4, 15, and 18 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclosed in the cited Baumert.

Claims 7, 18, and 31 depend from claims 1, 12, and 25, respectively, and further require indicating in the descriptor for the first packet a number of packets included in the buffer, including the first packet and the at least one subsequent packet that are transferred to the buffer with the first packet.

The Examiner cited the above discussed cols. 1, 3, and 5, as well as col. 6, lines 11-12 and element 74 and the sub-packet field as disclosing the additional requirements of these claims. (Office Action, pg. 9). Applicants traverse.

Applicants submit that the above discussed cols. 1, 3, and 5 nowhere disclose that the descriptor for the first packet indicates the number of packets included in the buffer.

The cited col. 6 mentions that descriptors point to the buffers which contain the received data packet. The cited element 74 in FIG. 4 shows a descriptor having a byte count and buffer address. The "subpacket" field refers to "a subpacket or subportion of a data packet, of buffer 70. Further, a new buffer may need to be allocated if the next subpacket of a packet requires a new 256 byte buffer. (Baumert, col. 8, lines 4-23). Thus, the subpacket field refers to the subpackets of a packet that fit into one or more buffers.

Nowhere does this cited Baumert anywhere disclose that the descriptor for one packet in memory indicates the number of packets included in the buffer when multiple packets are transferred to the buffer. Instead, the cited "subpacket" field in the descriptor of Baumert indicates the subpacket number of the packet that is stored in the buffer, where if the buffer size is too small for a packet, the packet's subpackets are stored in multiple buffers.

Accordingly, claims 7, 18, and 31 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclosed in the cited Baumert.

5. Claims 8, 19, and 32 are Patentable Over the Cited Art

The Examiner rejected claims 8, 19, and 32 as obvious (35 U.S.C. §103) over Baumert in view of Muthukrishan (U.S. Patent Pub. No. 2005/0135356). Applicants traverse for the following reasons.

Claims 8, 19, and 32 are patentable over the cited art because they depend from claims 1, 12, and 25, respectively, which are patentable over the cited art for the reasons discussed above.

Conclusion

For all the above reasons, Applicants submit that the pending claims 1-9, 12-20, and 23-33 are patentable over the art of record. Applicants submit herewith the fees for the two-month extension of time. Nonetheless, should any additional fees be required, please charge Deposit Account No. 50-0585.

The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

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